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		Application Number	10/075,086
		Filing Date	02/10/02
		First Named Inventor	Haw-minn Lu
		Art Unit	2666
		Examiner Name	Seema Srinivas Rao
Sheet 1	of 1	Attorney Docket Number	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
Rh		AGRAWAL, "Testing and Fault-Tolerance of Multistage Interconnection Networks," Computer, Apr. 1982, pp. 41-53, vol. 15, no. 4, IEEE, US	
		BHUYAN, et. al "Design and Performance of Generalized Interconnection Networks," IEEE Transactions on Computers, Dec. 1983, pp. 1081-1090, vol. 32, no. 12, IEEE, US	
		BLAKE, et. al "Multistage Interconnection Network Reliability," IEEE Transactions on Computers, Nov. 1989, pp. 1600-1603, vol. 38, no. 11, IEEE, US	
		CHIN, et. al "Packet Switching Networks for Multiprocessors and Data Flow Computers," IEEE Transactions on Computers, Nov. 1984, pp. 991-1003, vol. 33, no. 11, IEEE, US	
		KUMAR, et. al "Failure Dependent Performance Analysis of a Fault-Tolerant Multistage Interconnection Network," IEEE Transactions on Computers, Dec. 1989, pp. 1703-1713, vol. 38, no. 12, IEEE, US	
		TZENG, et. al "Realizing Fault-Tolerant Interconnection Network via Chaining," IEEE Transactions on Computers, Apr. 1988, pp. 458-462, vol. 37, no. 4, IEEE, US	
✓		VARMA, et. al "Fault-Tolerant Routing in Multistage Interconnection Networks," IEEE Transactions on Computers, Mar. 1989, pp. 385-393, vol. 38, no. 3, IEEE, US	

Examiner Signature	<i>Seema Srinivas Rao</i>	Date Considered	12/20/03
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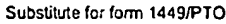
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